Diana Wofk

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Summary

I am a recent graduate of MIT working on energy-efficient learning-based vision for robotics applications. My experience and interests lie in algorithm-architecture-hardware co-design for efficient deployment of deep learning models on edge devices. I am excited about opportunities to work on ML/AI system design at the hardware-software interface.

Education

2018–2020 **Massachusetts Institute of Technology**, Master of Engineering, Electrical Engineering and Computer Science. Concentration in Computer Systems, *5.0/5.0*.
Thesis: Fast and Energy-Efficient Monocular Depth Estimation on Embedded Systems
Advisor: Prof. Vivienne Sze

2014–2018 **Massachusetts Institute of Technology**, Bachelor of Science, Electrical Engineering and Computer Science (Course 6-2), *5.0/5.0*.

2010–2014 **Stuyvesant High School**, Advanced Diploma with Honors, *98/100*.

Relevant Coursework

Hardware Architecture for Deep Learning; Digital Integrated Circuits; Digital Image Processing; Signals and Inference; Computation Structures; Computer System Engineering; Computer Systems Security

Professional Experience

2018-2020 **Research Assistant**, *Energy-Efficient Multimedia Systems Group*, **MIT**.
Advisor: Prof. Vivienne Sze
- Thesis [1] on algorithm and hardware design for fast and energy-efficient learning-based monocular depth estimation on embedded systems.
  - Explored deep neural network (DNN) simplification and compilation to enable real-time depth inference on the NVIDIA Jetson TX2 (178 fps) and iPhone X (40 fps).
  - Designed and implemented a custom dataflow and accelerator to reduce data movement and ensure high spatial utilization of hardware. On an Ultra96 FPGA, the DNN accelerator achieved 1.5-2× better energy-efficiency than the TX2 CPU.

2015-2018 **Undergraduate Researcher**, *Energy-Efficient Multimedia Systems Group*, **MIT**.
Advisor: Prof. Vivienne Sze
Mentors: Mehul Tikekar, Amr Suleiman, Tien-Ju Yang, Fangchang Ma
- Investigated tradeoffs between the computational complexity, runtime, and energy consumption of deep learning models for monocular depth estimation.
- Designed, built, and debugged communication interfaces between PCs (primarily running Linux), FPGAs, and embedded computing platforms.
  - Supported the PC-FPGA-chip interface as part of the group's Navion visual inertial odometry (VIO) system designed to demonstrate real-time processing on chip.
  - Interfaced an FPGA board to an NVIDIA Jetson TX1 via PCIe to demonstrate CNN-based super-resolution applied to compressed video during decoding.
  - Developed a PC-FPGA Ethernet interface that uses raw 1GbE for bulk data transfer to and from a Xilinx VC707. Explored and tested different methods of data flow control (stop-and-wait, credit-based). Final design achieved transfer speeds of 118 MBps.

2017 **Pre-Silicon Validation Intern**, *CPU Development Group*, **Intel**, Santa Clara, CA.
Manager: Julia Lin
Supervisor: Chandana Kanakamma
- Developed Python-based scripts to improve debug flow by automating log parsing and regression testing for errors in pre-silicon validation.

2016 **System ASIC Bring-Up Intern**, *IBM Systems*, **IBM**, Poughkeepsie, NY.
Manager: David Yearack
Supervisor: Mushfiq Saleheen
- Supported the bring-up of a chip part of the FICON/OSA adapter designed for a next-generation z System. Wrote shell scripts to automate system characterization (voltage, temperature, and frequency variation) on the test floor. Assisted with stress-testing I/O hardware in a z13 mainframe.

Awards and Honors

2018 SuperUROP Research Project Award, *MIT EECS*

2018 Certificate in Advanced Undergraduate Research, *MIT EECS*

2017 Analog Devices Undergraduate Innovation and Research Scholarship

2017 Certificate of Engineering Leadership, *Gordon-MIT Engineering Leadership Program*

2015 Excellence in German Studies – First Prize, *MIT Global Studies and Languages*

2014 AP National Scholar, *The College Board*

Publications

[1] **Diana Wofk**. Fast and Energy-Efficient Monocular Depth Estimation on Embedded Systems. MEng Thesis, Massachusetts Institute of Technology, 2020.
Discusses our work on the FastDepth DNN [2] achieving real-time inference on an embedded CPU/GPU and mobile phone. Proposes a custom-designed dataflow and accelerator architecture for running FastDepth layers on a low-power embedded FPGA. Explains our hardware-algorithm co-design approach, analyses tradeoffs (e.g. hardware reconfigurability vs. performance), and presents implementation results.

[2] **Diana Wofk***, Fangchang Ma*, Tien-Ju Yang, Sertac Karaman, Vivienne Sze. FastDepth: Fast Monocular Depth Estimation on Embedded Systems. In *IEEE International Conference on Robotics and Automation (ICRA)*, 2019.
Proposes an efficient and lightweight encoder-decoder deep neural network (DNN) for monocular depth estimation. Additionally discusses network compilation and network pruning targeting real-time inference on the NVIDIA Jetson TX2 embedded platform. Evaluation code and demo videos at http://fastdepth.mit.edu/.

Talks and Presentations

Talk "Fast and Energy-Efficient Monocular Depth Estimation on Embedded Systems." *MIT.nano Explorations Webinar Series*, July 2020.

Poster "Fast and Energy-Efficient Monocular Depth Estimation on Embedded Platforms." *MIT Microsystems Annual Research Conference*, January 2020.

Poster "Efficient Computing for Low Energy Robotics." *MIT College of Computing Launch Celebration – Poster Session*, February 2019.

Poster "Fast Monocular Depth Estimation on Embedded Systems." *MIT Microsystems Annual Research Conference*, January 2019.

Poster "Energy-Efficient Deep Neural Network for Depth Prediction." *MIT EECS SuperUROP Showcase*, April 2018. [video link]

Poster "Energy-Efficient Deep Neural Network for Depth Prediction." *MIT Microsystems Annual Research Conference*, January 2018.

Teaching Experience

Spring 2020 **Teaching Assistant**, MIT EECS.
6.033 Computer System Engineering [course website]

Fall 2019 **Teaching Assistant**, MIT EECS.
6.111 Introductory Digital Systems Lab [course website]

Fall 2018 **Teaching Assistant**, MIT EECS.
6.111 Introductory Digital Systems Lab [course website]

Fall 2017 **Lab Assistant**, MIT EECS.
6.111 Introductory Digital Systems Lab [course website]

Technical Reviewing

- 2020 IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS) Submission Reviewer.

Memberships

- Eta Kappa Nu (HKN), Beta Theta Chapter. *Inducted April 2017.*
- Tau Beta Pi (TBP), Mass Beta Chapter. *Inducted February 2017.*

Skills

Languages English, Russian, German

Coding Python, C, Bash, MATLAB, Verilog, SystemVerilog

Frameworks PyTorch, TVM

Design Tools Vivado Design Suite, Xilinx ISE, ModelSim